AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor integrated circuit comprising:

a first controlling circuit section ~~inputted with~~ having input thereto an input signal having an amplitude between a low voltage and the ground, said first controlling circuit operating with ~~the low voltage of~~ an electricity source of the low voltage, said first controlling circuit outputting ~~putting out~~ a first control signal generated by ~~said~~ the input signal, outputting ~~putting out~~ an inverse signal of the first control signal, and outputting ~~putting out~~ a second control signal generated from the first control signal[[,]];

a level transforming circuit having input thereto ~~inputted with said~~ the first control signal[[,]] ~~inputted with said~~ and the inverse signal, and outputting ~~putting out~~ a first signal having an amplitude between ~~said~~ the low voltage and a high voltage higher than ~~said~~ the low voltage[[,]];

a first buffer circuit ~~which has~~ having a first p-channel type MOS transistor connected between ~~said high voltage of~~ an electricity source of the high voltage and a first output node, wherein a gate of said first p-channel type MOS transistor is supplied with ~~said~~ the first signal, ~~and which has~~ said first buffer circuit having a first n-channel type MOS transistor connected between said first output node and the electricity source of the low voltage ~~ground~~, wherein a gate of said first n-channel type MOS transistor is supplied with ~~said~~ the first signal, and wherein said first buffer circuit outputs ~~puts out~~ a second signal having an amplitude between ~~said~~ the high voltage and ~~said~~ the low voltage to said first output node;

a second buffer circuit ~~which has~~ having a second p-channel type MOS transistor connected between ~~said low voltage of~~ the electricity source of the low voltage and a second output node, wherein a gate of said second p-channel type MOS transistor is supplied with ~~said~~ the second control signal, said second buffer circuit having a ~~and which has~~ second n-channel type MOS transistor connected between said second output node and the ground, wherein a gate of said second n-channel type MOS transistor is supplied with the ~~said~~ second control signal, and wherein said second buffer circuit ~~puts out~~ outputs a third signal having an amplitude between ~~said~~ the low voltage and the ground to said second output node; and

an overvoltage protecting circuit ~~which has~~ having a drain of ~~said~~ a third p-channel type MOS transistor connected with a third output node, wherein a source of said third p-channel type MOS transistor is supplied with ~~said~~ the second signal, said overvoltage protecting circuit having ~~and which has~~ a drain of ~~said~~ a third n-channel type MOS transistor connected with said third output node, wherein a source of said third n-channel type MOS transistor is supplied with ~~said~~ the third signal, and wherein each gate of said third p-channel type MOS transistor and said third n-channel type MOS transistor is supplied with ~~said~~ the low voltage in common, and ~~puts out~~ wherein said overvoltage protecting circuit outputs a fourth signal having an amplitude between ~~said~~ the high voltage and the ground to said third output node.

2. (Currently Amended) A semiconductor integrated circuit according to Claim 1[[:]],

further comprising a pre-buffer circuit connected with the output of said level transforming circuit, wherein said pre-buffer circuit outputs the ~~so as to put out said~~ first signal having an amplitude between the high voltage and the low voltage.

3. (Currently Amended) A semiconductor integrated circuit according to Claim 2[[:]], wherein said pre-buffer circuit adjusts a timing of inputting said first buffer circuit with ~~said~~ the first signal.

4. (Currently Amended) A semiconductor integrated circuit according to Claim 1[[:]],

wherein a turning on resistance of said first p-channel type MOS transistor in said first buffer circuit is set higher than a turning on resistance of said third p-channel type MOS transistor, and

wherein a turning on resistance of said second n-channel type MOS transistor in said second buffer circuit is set higher than a turning on resistance of said third n-channel type MOS transistor in said overvoltage protecting circuit.

5. (Currently Amended) A semiconductor integrated circuit according to Claim 1[[:]],

wherein a substrate ~~substrates~~ of said first n-channel type MOS transistor in said first buffer circuit is connected with a source of said first n-channel type MOS transistor, and a substrate of said third n-channel type MOS transistor in said overvoltage protecting circuit is connected with said source of said third n-channel type MOS transistor[[;]],

wherein said substrate of said first n-channel type MOS transistor and said substrate of said third n-channel type MOS transistor are isolated from a substrate of said second n-channel type MOS transistor.

6. (Currently Amended) A semiconductor integrated circuit according to Claim 1[[:]],

wherein a substrate of said third p-channel type MOS transistor is connected with said source of said third p-channel type MOS transistor, and is isolated from substrates of said first and second p-channel type MOS ~~transistor~~ transistors.

7. (Currently Amended) A semiconductor integrated circuit according to Claim 1[[:]],

wherein said p-channel type MOS transistors and said n-channel type MOS transistors are formed on an active region isolated by an insulating film.

8. (Currently Amended) A semiconductor integrated circuit comprising:

a first controlling circuit section ~~inputted with~~ having input thereto a data input signal having an amplitude between a low voltage and the ground, and having input thereto ~~inputted with~~ an enable signal, said first controlling circuit operating with ~~the low voltage of~~ an electricity source of the low voltage, said first controlling circuit outputting ~~putting out~~ a first control signal generated by ~~said~~ the data input signal and ~~said~~ the enable signal, outputting ~~putting out~~ a first inverse signal of the first control signal, outputting ~~putting out~~ a second control signal generated by ~~said~~ the data input signal and ~~said~~ the enable signal, outputting ~~putting out~~ a second inverse signal of the second control signal, outputting ~~putting out~~ a third control signal generated from

the first control signal, and outputting ~~putting out~~ a fourth control signal generated from the second control signal[[,]];

a first level transforming circuit having input thereto the ~~inputted with said~~ first control signal[[,]] and the ~~inputted with said~~ first inverse signal, and outputting ~~putting out~~ a first signal having an amplitude between ~~said~~ the low voltage and a high voltage higher than ~~said~~ the low voltage[[,]];

a second level transforming circuit having input thereto the ~~inputted with said~~ second control signal[[,]] and the ~~inputted with said~~ second inverse signal, and outputting ~~putting out~~ a second signal having an amplitude between ~~said~~ the low voltage and a high voltage higher than ~~said~~ the low voltage[[,]];

a first buffer circuit having a ~~which has~~ first p-channel type MOS transistor gate of said first p-channel type MOS transistor supplied with ~~said~~ the first signal, said first p-channel type MOS transistor connected between ~~said high voltage of~~ the electricity source of the high voltage and a first output node, said first buffer circuit having a ~~and which has~~ first n-channel type MOS transistor gate of said first n-channel type MOS transistor supplied with ~~said~~ the second signal, said first n-channel type MOS transistor connected between said first output node and the electricity source of the low voltage ~~ground~~, and wherein said first buffer circuit outputs ~~puts out~~ a third signal having an amplitude between ~~said~~ the high voltage and ~~said~~ the low voltage to said first output node;

a second buffer circuit having a ~~which has~~ second p-channel type MOS transistor gate of said second p-channel type MOS transistor supplied with ~~said~~ the third control signal, said second p-channel type MOS transistor connected between ~~said low voltage of~~ the electricity source of the low voltage and a second output node, said second buffer circuit having a ~~and which has~~ second n-channel type MOS transistor gate of said second n-channel type MOS transistor supplied with ~~said~~ the fourth control signal, said second n-channel type MOS transistor connected between said second output node and the ground, and wherein said second buffer circuit outputs ~~puts out~~ a fourth signal having an amplitude between ~~said~~ the low voltage and the ground to said second output node; and

an overvoltage protecting circuit having a ~~which has~~ third p-channel type MOS transistor source of said third p-channel type MOS transistor supplied with ~~said~~ the third signal, wherein a drain of said third p-channel type MOS transistor is connected with a third output node, said overvoltage protecting circuit having a ~~and which has~~ third n-channel type MOS transistor source of said third n-channel type MOS transistor supplied with ~~said~~ the fourth signal, wherein a drain of said third n-channel type MOS transistor is connected with said third output node, ~~and~~ wherein each gate of said third p-channel type MOS transistor and said third n-channel type MOS transistor is supplied with ~~said~~ the low voltage in common, and wherein said overvoltage protecting circuit outputs ~~puts out~~ a fifth signal having an amplitude between ~~said~~ the high voltage and the ground to said third output node.

9. (Currently Amended) A semiconductor integrated circuit according to Claim 8[[:]],

further comprising a pre-buffer circuit connected with the output of said level transforming circuit, wherein said pre-buffer circuit outputs the ~~so as to put out said~~ first signal having an amplitude between the high voltage and the low voltage.

10. (Currently Amended) A semiconductor integrated circuit according to Claim 9[[:]],

wherein said pre-buffer circuit adjusts a timing of inputting said first buffer circuit with ~~said~~ the first signal.

11. (Currently Amended) A semiconductor integrated circuit according to Claim 8[[:]],

wherein a turning on resistance of said first p-channel type MOS transistor in said first buffer circuit is set higher than a turning on resistance of said third p-channel type MOS transistor, and

wherein a turning on resistance of said second n-channel type MOS transistor in said second buffer circuit is set higher than a turning on resistance of said third n-channel type MOS transistor in said overvoltage protecting circuit.

12. (Currently Amended) A semiconductor integrated circuit according to Claim 8[[:]],

wherein a substrate ~~substrates~~ of said first n-channel type MOS transistor in said first buffer circuit is connected with a source of said first n-channel type MOS transistor, and a substrate of said third n-channel type MOS transistor in said overvoltage protecting circuit is connected with said source of said third n-channel type MOS transistor[[;]],

wherein said substrate of said first n-channel type MOS transistor and said substrate of said third n-channel type MOS transistor are isolated from a substrate of said second n-channel type MOS transistor.

13. (Currently Amended) A semiconductor integrated circuit according to Claim 8[[:]],

wherein a substrate of said third p-channel type MOS transistor is connected with said source of said third p-channel type MOS transistor, and is isolated from substrates of said first and second p-channel type MOS ~~transistor~~ transistors.

14. (Currently Amended) A semiconductor integrated circuit according to Claim 8[[:]],

wherein said p-channel type MOS transistors and said n-channel type MOS transistors are formed on an active region isolated by an insulating film.